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The diagram illustrates the TTPB system architecture, enclosed in a dashed box. The components and their interconnections are as follows:

- PL (Program Loader)**: Connected to the **LI (Local Interface)**.
- LI (Local Interface)**: Connected to the **CU (Control Unit)** and the **EU (Execution Unit)**.
- LS (Local Storage)**: Connected to the **CU**.
- CU (Control Unit)**: Connected to the **EU** and the **CDR (Control Data Register)**.
- EU (Execution Unit)**: Connected to the **CU**, the **CDR**, and the **PCR (Program Counter Register)**.
- CDR (Control Data Register)**: A vertical stack of three registers labeled **D**, **C**, and **S**. It has multiple input/output lines on its left side.
- RTC (Real-Time Clock)**: Connected to the **GU (General Purpose Register)**.
- GU (General Purpose Register)**: Connected to the **CDR** and the **SRN (Serial Register Network)**.
- SRN (Serial Register Network)**: Connected to the **GU** and the **PCR**.
- PCR (Program Counter Register)**: Connected to the **EU** and the **SRN**.
- DATA** and **H-DATA** buses: These buses connect the system to the **RD (Read Data)** block outside the dashed box.